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Programmable High-Output-Impedance, Large-Voltage Compliance, Microstimulator for Low-Voltage Biomedical Applications

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Abstract— **This paper reports on the design of a programmable, high output impedance, large voltage compliance microstimulator for low-voltage biomedical applications. A 6-bit binary-weighted digital to analog converter (DAC) is used to generate biphasic stimulus current pulses. A compact current mirror with large output voltage compliance and high output resistance conveys the current pulses to the target tissue. Designed and simulated in a standard 0.18µm CMOS process, the microstimulator circuit is capable of delivering a maximum stimulation current of 160µA to a 10-kΩ resistive load. Operated at a 1.8-V supply voltage, the output stage exhibits a voltage compliance of 1.69V and output resistance of 160MΩ at full scale stimulus current. Layout of the core microelectrode circuit measures 25.5µm×31.5µm.**

I. Introduction

Nowadays, there is a great demand for using neuroprosthetic devices and neural stimulators to effectively treat disabilities and neurological disorders such as blindness, Parkinson's disease, and spinal cord injury [1-3].

A neural stimulator is in charge of generating electrical stimulation pulses and delivering them to the target tissue. In general, electrical stimulation of excitable cells can be performed in one of the following forms:

– Voltage-controlled stimulation (VCS), in which a voltage pulse is applied to the target tissue. A main drawback for this approach is that the current passing through the tissue is highly dependent on the electrode or tissue impedance. Therefore, the charge delivered to the tissue is not well controlled. The VCS form is suitable for power-efficient circuits [4].

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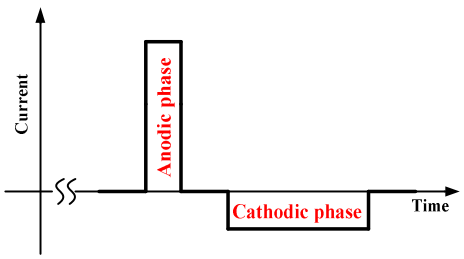

Figure 1. A typical biphasic current pulse

– Current-controlled stimulation (ICS), in which a current pulse is applied to the target tissue. In this form of electrical stimulation, the stimulus current passes through the tissue regardless of the tissue impedance. Using this approach better control over the stimulus current and also safer stimulation is achieved [5, 10].

– Charge-controlled stimulation (QCS), in which the charge injected into the target tissue is controlled. The main drawback of this method is large chip-area occupied due to the many capacitors employed [6].

There are two general stimulus current waveforms used in neural stimulation: a *monophasic pulse* and a *biphasic pulse*. Monophasic stimulation causes charge accumulation at the electrode-tissue interface and leads to tissue damage. In charge balanced biphasic stimulation, each pulse is followed by a pulse of reverse polarity and results in no residual charge on the electrode and prevents tissue damage. Biphasic stimulation is widely used in the neural stimulators and is shown in Fig. 1 [5, 7, and 10].

From a circuit design point of view, since the site and tissue impedance are variable over time [8, 9], it is important to have a high-output-impedance output stage for a microstimulator. This is to maintain a constant stimulus current during the stimulation. A conventional way to enhance the output impedance is to increase the channel length of the output transistors. Voltage compliance for the output stage is lowered by increasing the channel width of the output transistors. This, however, leads to have a large chip area, which is not welcomed in implantable microstimulators.

In this paper, a microstimulator is presented, which is capable of providing high output impedance and large voltage compliance under low supply voltage while occupying small chip area. The proposed microstimulator is designed for neural interfacing applications.

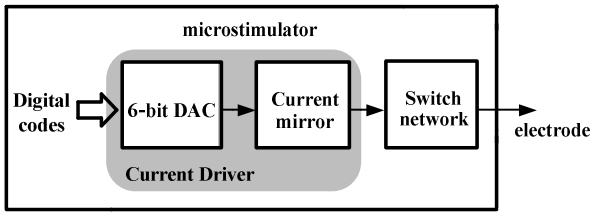

Figure 2. Conceptual block diagram of the proposed microstimulator

II. MICROSTIMULATOR ARCHITECTURE

In this work, the ICS method was preferred to the other two methods described in the previous section (i.e., VCS & QCS) for the generation of stimulation pulses. Conceptual block diagram of the microstimulator proposed in this work is shown in Fig. 2. The microstimulator is composed of two main parts: a *current driver*, which is composed of a digital-to-analog converter (DAC) and a current mirror, and a *switch network*. The high-performance current mirror conveys the stimulus current to a switch network. The switch network is used to make biphasic pulses by changing the direction of current flow through the target tissue, as required.

A. Compact High- Performance Current Mirror

Figure 3 shows the circuit schematic of the current mirror proposed in this work. The proposed current mirror fulfills the key requirements for microstimulation applications including low-voltage operation, high output impedance, and large voltage compliance. In this circuit, a single-ended folded cascode amplifier is used as a compact amplifier to not only boost the output impedance of the current mirror, but also reduce silicon area and power consumption compared with some of the schemes reported in the literature [10]. This amplifier comprises transistors M_8, M_9 and M_{b7}, M_{b8} performing each as a current source. The DC level-shifter, M_6, is used to lower and also set the DC level at the input of the proposed current mirror. The differences between the gate-source voltages of transistors (M_5, M_6) and (M_7, M_8) define the drain-source voltages of transistors M_1 and M_2, respectively. Symmetric design of both sides of the current mirror forces the drain-source voltages of transistors M_1 and M_2 to be equal, leading to improvement in the current copying accuracy and also the linearity of the circuit. In this circuit, input current is injected into the source of transistor M_3 instead of its drain. This technique has two advantages: (a) it lowers the minimum input voltage to the difference between the gate-source voltages of M_1 and M_2, and (b) it reduces the input impedance by the gain of transistor M_3 due to the shunt feedback provided by M_3 [11]. To enhance the voltage compliance of the current mirror, M_1 and M_2 are biased to operate in the linear region. This leads to reduction in drain-source voltages of these transistors and consequently improvement in the voltage compliance of the circuit. This topology for the current mirror, however, lowers the output impedance compared to a regular cascode current mirror. To overcome this problem, the output impedance is boosted by a negative feedback mechanism applied using a single-stage folded cascode amplifier. Output impedance of the current mirror is given as:

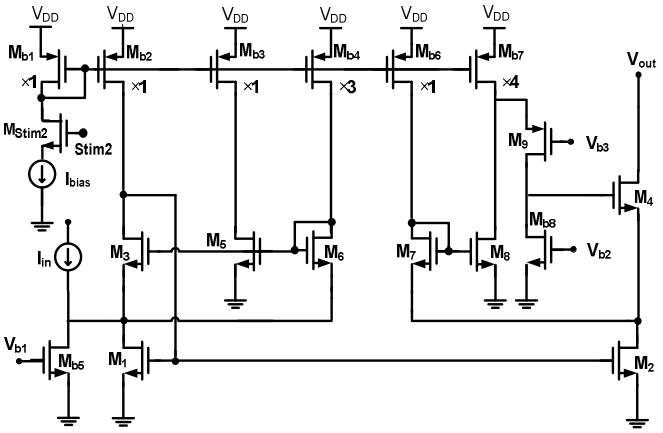

Figure 3. Circuit schematic of the proposed current mirror

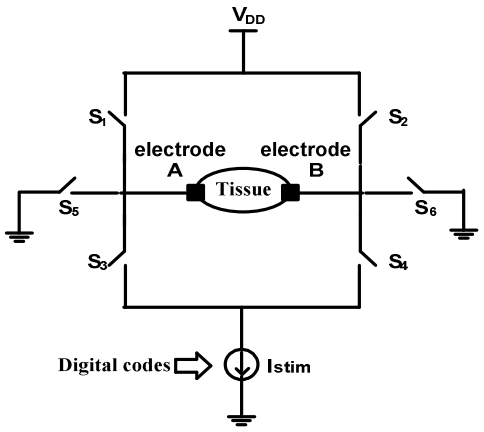

Figure 4. Conceptual diagram of the biphasic current generation

$$R_{out} = A\, g_{m_4} r_{ds_4} r_{ds_2} \quad (1)$$

where A is the gain of the single-ended folded cascode amplifier:

$$A = g_{m_8} [r_{ds_{mb8}} \,||\, [(r_{ds_8} \,||\, r_{ds_{mb7}})(1 + g_{m_9} r_{ds_9}) + r_{ds_9}]] \quad (2)$$

It can be shown that the input resistance of the current mirror is calculated as:

$$R_{in} = \frac{1}{g_{m_1} g_{m_3} r_{ds_3}} \quad (3)$$

The transistor M_{stim2} is used to turn off the current mirror while not stimulating. This is to conserve the power dissipation of the proposed microstimulator in standby mode.

B. Switch Network Configuration

To generate biphasic stimulation current pulses out of a constant current provided by a simple current source/mirror, a switch network is usually used. Fig. 4 shows the switch network used in the stimulation back-end of this work. Arranged in a bridge-like configuration, switches S_1-S_4 are in charge of the generation of biphasic current pulses. This scheme is used in power- and area-efficient configurations where a single current source is used and the entire

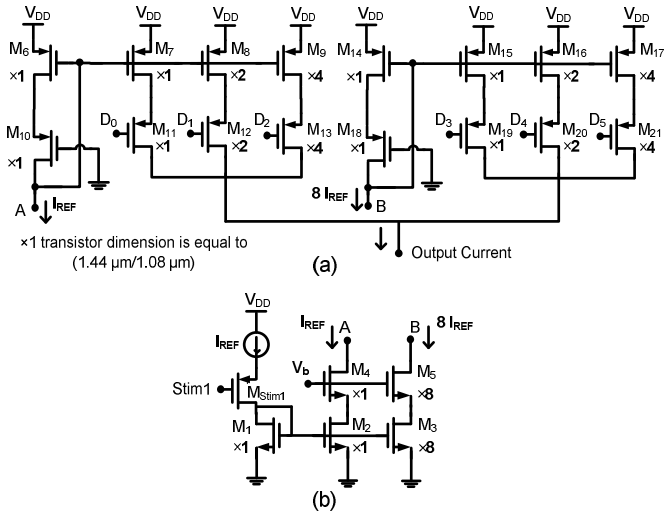

Figure 5. The proposed DAC (a) circuit schematic, (b) reference current generator

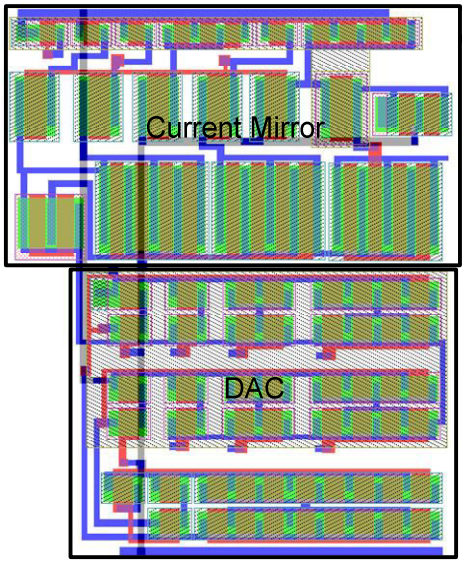

Figure 6. Core chip-layout of the microstimulator

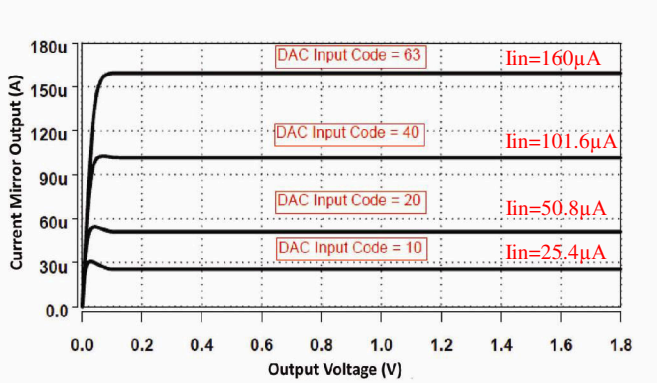

Figure 7. DC output characteristics of the proposed current mirror

stimulation back-end operates under a single-rail supply voltage. Switches S_5 and S_6 are envisioned for grounding the stimulation sites. This is to provide a path for discharging any residual charge due to the mismatch between the two opposite phases (anodic and cathodic phases) to prevent tissue damage.

C. Digital-to-analog converter

An accurate low-voltage binary-weighted 6-bit current-mode DAC is used in the proposed microstimulator to generate the desired stimulus current. Figure 5 shows the proposed DAC circuit, in which all the transistors operate in the saturation region. As shown in Fig. 5(b), the reference current I_{ref} =2.54µA provided by a current reference circuit is mirrored into transistors M_2 and M_3. With the dimensions shown on the circuit, the drain current of M_3 is 8 times larger than that of M_2. Choosing identical dimensions for M_4 and M_5 with the transistors M_2 and M_3 respectively, leads to have equal drain-source voltages for the transistors M_2 and M_3. This is to improve current copying accuracy of the circuit. As shown in Fig. 5(a), drain currents of M_4 and M_5 are mirrored by the transistors M_6 and M_{10} to the left and right sides of the DAC, respectively. It should be highlighted that, realizing a 6-bit binary-weighted DAC using identical dimensions for transistors in both sides, leads to save significant chip-area. The transistor M_{stim1} is used to turn off the DAC when no current pulse is generated. This is to save power when the proposed microstimulator is in the inactivate mode. By turning M_{stim1} on, the total output current of the DAC is controlled by the digital bits (D_0-D_5). The total output current of the DAC is expressed as:

$$I_{out} = I_{ref}(D_0 + 2D_1 + 2^2 D_2 + 2^3 D_3 + 2^4 D_4 + 2^5 D_5) \quad (4)$$

III. SIMULATION RESULTS

Figure 6 shows a core-chip layout of the proposed neural microstimulator developed in a 0.18µm standard N-well CMOS process. Core of the microstimulator occupies a silicon area of 25.5µm×31.5µm. In the *standby mode*, when M_{stim1} and M_{stim2} are off, the DAC input code is equal to zero, and the microstimulator consumed almost no current. Operated under 1.8V power supply and with a bias current of I_{bias}=10µA, the microstimulator circuit consumes 816µW when delivering the full-scale stimulus current of 160µA to a 10KΩ resistive load. Fig. 7 shows the DC output characteristics of the current mirror for the input current (I_{in}) of 25.4µA, 50.8µA, 101.6µA, and 160µA. Specifications of the circuit are summarized in Table I. Figure 8 shows the simulated stimulus output current versus the input digital codes of the DAC. According to simulations, the DAC was

TABLE I
SPECIFICATION OF THE PROPOSED CURRENT MIRROR

parameter	Iin = 25.4μA	50.8μA	101.6μA	160μA
Iout	24.66	50.12	101	159.26
Output Resistance	1.2$G\Omega$	813$M\Omega$	325$M\Omega$	160$M\Omega$
Voltage Compliance	1.73V	1.72V	1.7V	1.69V
Power Consumption	227μW	258μW	319μW	388μW

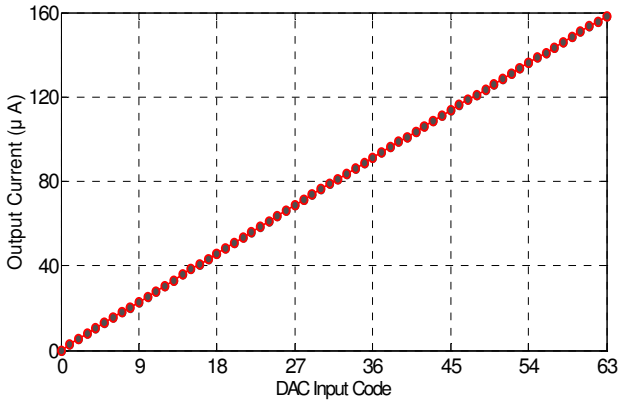

Figure 8. Stimulus output current versus DAC input codes

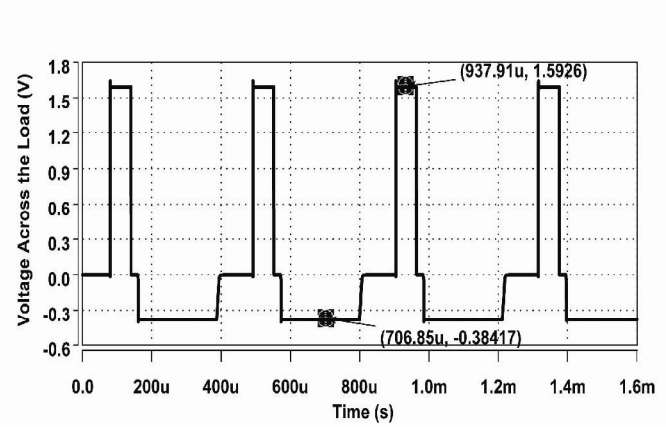

Figure 9. A train of biphasic stimulation pulses

TABLEL II
PERFORMANCE COMPARISON WITH OTHER STIMULATORS

Specification	[10]	[12]	This work
Supply Voltage	5V	3V	1.8V
Full Scale Current	94.5μA	259μA	160μA
Resolution	6 Bits	N/A	6 Bits
Maximum INL(LSB)	0.47LSB	N/A	0.4LSB
Voltage Compliance	94%V_{DD}	87%V_{DD}	94%V_{DD}
Output Resistance	>45MΩ	N/A	160MΩ
Area	0.022mm^2	0.02mm^2	0.0007mm^2
Technology	0.35μm	0.35μm	0.18μm
Power Consumption	945μW	750μW	816μW

found to have a simulated integral nonlinearity (INL) equal to ±0.4 LSB. The microstimulator is capable of providing 1.69V voltage compliance under a 1.8V voltage supply at the maximum deliverable stimulus current of 160μA. At this current, output impedance of the circuit is 160MΩ. Figure 9 shows an example of the generation of biphasic stimulus current pulses. Performance comparison between the proposed microstimulator circuit and two other stimulators recently reported are presented in Table II. All the specifications for this work in Table II are calculated for the full-scale current case.

IV. CONCLUSIONS

In this paper, a programmable, high output impedance, high voltage compliance, microstimulator is presented, which is capable of operating in low voltage biomedical applications. Biphasic current-controlled pulses are generated with digitally-controlled amplitudes for both anodic and cathodic phases. The proposed microstimulator is designed to operate as a SFE (stimulation-front-end) part of a neural prosthesis.

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